WHAT IS CLAIMED IS:

1. A circuit for controlling signal levels on a transmission channel, comprising:

a voltage divider to output an average of its inputs;

a first output driver connected to a first input of the voltage divider;

a second output driver connected to a second input of the voltage divider;

an input comparator to compare the output of the voltage divider with a reference voltage;

a latch to sample an output of the input comparator;

a current control counter holding a current control value, adjusted based on a content of the latch, wherein the current control counter determines output levels at an output of the integrated circuit.

2. The circuit of claim 1 further comprising:

an isolation block to shield interaction between the voltage divider and an output pad during a period when current levels are not being evaluated at the output of the integrated circuit.

3. The circuit of claim 1 wherein the current control counter is an up/down counter.

4. A circuit for controlling signal levels on a transmission channel, comprising:

a comparator with a reference voltage input node, a current control voltage input node, and an output node;

a voltage divider with a first input node connected to a termination resistor node, a second input node connected to said termination resistor node, and an output node connected to said current control voltage input node;

a first output driver circuit connected to said first input node to control the value thereon;

a second output driver circuit connected to said second input node to control the value thereon; and

a current control circuit connected to said comparator output node, said current control circuit controlling signal levels on a transmission channel in response to an output signal from said comparator.

5. The circuit of claim 4 wherein said current control circuit is an up/down counter.

6. A circuit for controlling the operating current of an output driver, comprising:

a first adjustable output driver responsive to a current setting input signal;

a second adjustable output driver responsive to said current setting input signal;

a first load element with one end coupled to a termination voltage and a second end coupled to said first adjustable output driver;

a second load element with one end coupled to a termination voltage and a second end coupled to said second adjustable output driver;

a voltage divider with a first input node, a second input node, and a common node, said common node providing an output voltage based upon signals received at said first input node and said second input node;

a first signal link between said first input node and said first adjustable output driver;

a second signal link between said second input node and said second adjustable output driver;

a comparator to produce a comparator output signal based upon a reference voltage and said output voltage from said voltage divider; and

a counter to generate said current setting input signal in response to said comparator output signal, such that said output voltage of said voltage divider is substantially the same as said reference voltage.

7. The circuit of claim 6 further comprising a latch to store the comparator output signal during normal operation.

8. The circuit of claim 6 further comprising a combinational and sequential logic circuit to filter said comparator output signal.

9. The circuit of claim 6 wherein said counter is an up/down counter.

10. The circuit of claim 6 further comprising a time-multiplexed common pin coupled to said first adjustable output driver, said second adjustable output driver, said first load element, and said second load element.

11. The circuit of claim 6 wherein said first load element and said second load element are each a linear resistor.

12. The circuit of claim 6 wherein said first load element and said second load element are each a non-linear device.

13. The circuit of claim 6 wherein said first output driver comprises a plurality of transistors of preselected widths arranged in a geometric manner.

14. The circuit of claim 6 wherein said first output driver comprises a plurality of transistors of preselected widths arranged in a logarithmic manner.

15. The circuit of claim 6 wherein said first output driver comprises a plurality of transistors of preselected widths arranged in linear manner.

16. The circuit of claim 6 wherein said first output driver comprises a plurality of transistors of preselected widths arranged in non-linear manner.

17. The circuit of claim 6 wherein said voltage divider is a resistive ladder.

18. The circuit of claim 6 wherein said voltage divider has selectable divide ratios.

19. The circuit of claim 6 wherein said voltage divider is a digital-to-analog converter.

20. The circuit of claim 6 wherein said voltage divider is a switched capacitor processor.

21. The circuit of claim 6 wherein said voltage divider is a digital signal processor.

22. The circuit of claim 6 wherein said voltage divider is a resistive ladder.

23. The circuit of claim 6 wherein said first signal link and said second signal link are each a wire.

24. The circuit of claim 6 wherein said first signal link and said second signal link are each a semiconductor pass gate.

25. The circuit of claim 6 wherein said first signal link and said second signal link are each an operational amplifier buffer.

26. The circuit of claim 6 wherein said first signal link and said second signal link are each an analog-to-digital converter.

27. The circuit of claim 6 wherein said first signal link and said second signal link are each a capacitor.

28. The circuit of claim 6 wherein said first signal link and said second signal link are each a sample-and-hold circuit.

29. The circuit of claim 6 wherein said comparator is an analog comparator.

30. The circuit of claim 6 wherein said comparator is a digital signal processor.

31. The circuit of claim 6 wherein said first adjustable output driver, said second adjustable output driver, said first load element, said second load element, said voltage divider, said first signal link, said second signal link, said comparator, and said counter are positioned in a single package.

32. The circuit of claim 6 wherein said first adjustable output driver, said second adjustable output driver, said first load element, said second load element, said voltage

divider, said first signal link, said second signal link, and said comparator are positioned in a first package and said counter is positioned in a second package.

33. The circuit of claim 6 wherein said first adjustable output driver, said second adjustable output driver, said first load element, said second load element, said first signal link, and said second signal link are positioned in a first package and said voltage divider and said counter are positioned in a second package.

34. A method of establishing an operating current for an output driver, said method comprising the steps of:

coupling a voltage divider between two adjustable output drivers, wherein the first output driver is in an on state and the second is in an off state, and an output of each output driver is coupled to one side of a termination load device, while the other side of each termination load device is coupled to a termination voltage;

comparing a common node of said voltage divider to a reference voltage; and

adjusting the count value of a counter in response to said comparing step until said common node of said voltage divider is substantially the same as said reference voltage.